REMARKS

This is in response to the Office Action mailed on October 3, 2003 in which claims 2-6 and 8-14 were pending. In the Office Action, claims 6 and 8-13 were rejected under 35 U.S.C. §102(e) as being anticipated by Francis et al. (U.S. Patent No. 6,482,681), and claims 2, 3, 4, 5, and 14 were rejected under 35 U.S.C. §103(a) as being unpatentable over Francis et al. With this amendment, claim 1 is canceled without prejudice and claim 9 is amended. All of pending claims 2-6 and 8-14 are in condition for allowance. Reconsideration and notice to that effect is respectfully requested.

With regard to the rejections to claims 6 and 8-13, Francis et al. teach the formation of an insulated gate bipolar transistor (IGBT) including an n^+ buffer layer and a weak backside emitter formed on an n^- monocrystalline (normally FZ) wafer (i.e., non-epi). According to Francis et al., the formation of the IGBT device, and in particular the intersection of the P^+ region and the N^+ gradient curve, using present day equipment, is too variable to precisely control the forward voltage drop (V_{ce}) and speed of the device. This problem is solved, according to Francis et al., by forming the n^+ buffer layer via *implantation of hydrogen ions in the bottom of the thinned wafer* to control the concentration of the n^+ buffer at the bottom surface. The implantation of hydrogen ions is therefore performed after thinning of the backside of the wafer.

Francis et al. further teach that a diffused wafer can be used to create a punch-through IGBT, with the n^+ buffer being diffused just prior to complete backside thinning of the wafer (after the frontside structure of the wafer is complete). However, Francis et al. go on to explain that the diffused wafer results in a device having uncontrollable performance characteristics, which is undesirable. See col. 5, line 47 - col. 6, line 2. Furthermore, the diffusion of Francis et al. can have a severe effect on the completed frontside of the device because of the fact that this diffusion is performed at high temperatures (more than 1000°C), resulting in further unpredictability in the device's performance.

With this Amendment, claim 9 is amended. Previously presented claim 6 and amended claim 9 require fabricating from a uniformly-doped monocrystalline n^- starting wafer a nonuniformly doped n-type substrate which contains an n^- layer on a frontside of the wafer and a diffused n^+ layer

on a backside of the wafer, wherein the diffused n^+ layer is formed in the first step. The diffused layer is formed in the first step of this procedure when certain n-type dopant is heavily diffused into both sides of an n^- substrate at the same time. One (on the final frontside) of the two diffused layers is then removed by grinding and the exposed surface of the n^- substrate is further ground and polished to a proper position according to the required voltage rating of the device, thus the nonuniformly-doped substrate containing a diffused n^+ layer (on the final backside) is achieved. The doping concentration decays from the backside to the frontside. By fabricating the diffused n^+ layer in the first step, adverse effects which may occur to the frontside structure during high temperature processes (more than 1000 °C) are avoided. Forming the n^+ buffer layer *after* fabrication of the frontside structure and/or after thinning of the backside of the wafer, as is taught by Francis et al., may result in the frontside structure being destroyed during high temperature processes.

As discussed above, Francis et al. do not teach forming a diffused n^+ layer in the first step of fabrication. The primary teaching of Francis et al. is to implant hydrogen ions in the bottom of a wafer whose backside has already been thinned. This embodiment does not involve diffusion as claimed, and does not form the n^+ layer in the first step of fabrication. An alternative teaching of Francis et al. is to diffuse an n^+ buffer layer just prior to complete backside thinning of the wafer, after the frontside structure of the wafer is complete. Francis et al. teach that this embodiment is not desirable because of its inability to precisely control important performance characteristics of the resulting device. However, regardless of the desirability of this embodiment, the recitations of the claims are still not satisfied because the diffusion of the n^+ layer is performed after the frontside structure of the wafer is complete, not in the first step of fabrication as recited by the claims. Therefore, because Francis et al. does not teach or fairly suggest forming a low power loss semiconductor switching device including a diffused n^+ layer on a backside of the wafer formed in the first step of fabrication, the recited elements of independent claims 6 and 9 are not disclosed by the prior art and the rejections under 35 U.S.C. § 102(e) should accordingly be withdrawn.

Claims 8 and 10-13 were also rejected under 35 U.S.C. § 102(e) as being anticipated by Francis et al. Claim 8 depends from claim 6 and claims 10-13 depend directly or indirectly from

claim 9. As discussed above, claims 6 and 9 are not anticipated or otherwise taught by Francis et al. Therefore, claims 8 and 10-13 are also not anticipated or otherwise taught by Francis et al.

Claims 2-5 and 14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Francis et al. As discussed above, claims 6 and 9 are now in a condition for allowance. Claims 2-5 depend from allowable claim 6, and claim 14 depends from allowable claim 9. These claims are also allowable, since any claim depending from a patentable independent claim is also patentable. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

CONCLUSION

In view of the foregoing, all pending claims 2-6 and 8-14 are in condition for allowance. A notice to that effect is respectfully requested.

Entry of this Amendment after final rejection is appropriate because it places all of the pending claims in condition for allowance. In addition, the amendment made to independent claim 9 does not change the scope of claim 9 in such a way that would require a new search, since the step of forming a diffused n^+ layer in the first step of fabrication recited in amended claim 9 was already set forth in independent claim 6, which has already been searched and considered by the Examiner.

The Examiner is cordially invited to contact the undersigned at the telephone number listed below if such a call would in any way facilitate the allowance of this application.

Respectfully submitted,
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